REMARKS

Claims 1- 21 remain pending in this application with claim 3 being formally amended by this response.

Applicant's Representative would like to thank the Examiner for the courtesy extended during the telephone interview on December 4, 2006. During the telephone interview, Applicant's Representative presented arguments distinguishing the claimed "integrated circuit die for a flip chip" from the chip arrangements disclosed by Yamada and Tanaka, alone or in combination with one another. The arguments presented during the telephone interview are stated hereinbelow with respect to the Rejection of claims 1 – 21 under 35 USC 103(a). During the discussion between Applicant's Representative and Examiner Huynh, Examiner Huynh agreed that the present claimed invention is patentable over Yamada and Tanaka, both alone and in combination with one another. Thus, Examiner Huynh agreed that the present claimed invention was allowable pending a further search. Examiner Huynh further agreed to provide an Interview Summary with either a Notice of Allowance or any subsequent Office Action necessitated by the further search.

Objection to Claim 3

Claim 3 is objected to because the term "bond pad spacing" should read "bond pad pitch". Claim 3 is formally amended in accordance with the Examiner's suggestion. In view of these formal amendments to claim 3, Applicant respectfully submits that this objection has been satisfied and should be withdrawn.

Rejection of Claims 1-5, 8-12 and 15-19 under 35 U.S.C. 102(b)

Claims 1-5, 8-12 and 15-19 are rejected under 35 U.S.C. 102(b) as being unpatentable over Yamada et al. (US 6,121,690) in view of Tanaka et al. (US 5,216,280).

The present claimed invention provides an integrated circuit die for a flip chip. The integrated circuit includes a die and a plurality of die bond pads situated on the die. The die bond pads are situated in rows with every other row having a bond pad pitch different than that of a bond pad pitch of an adjacent row. The pitch of a row is defined by the length of a corresponding bond pad and the spacing therein between. Claims 1, 8 and 15 contain features similar to those discussed above.

"The size of the die is the primary driver of cost for an integrated circuit...Ways to reduce the amount of the die spent on these power busses could help reduce the size, and therefore the cost, of the die" (Page 2, lines 14-18). Therefore, the present claimed invention "takes into account the routing capabilities of the PCB and spaces every other row of bond pads such that two lines can be routed from every other row of bond pads and between the outer row of bond pads thereto. This provides a staggered spacing for the bond pads" (Page 4, lines 26-29).

Applicant notes the Rejection on page 3 agrees that Yamada neither discloses nor suggests that the die bond pads are situated in rows with every other row having a bond pad pitch different than that of a bond pad pitch of an adjacent row, wherein the pitch of a row is defined by length of a corresponding bond pad and the spacing therein between.

The Rejection cites Tanaka as disclosing this feature thus obviating the combination of the references. Specifically, the Rejection cites Figures 9 and 10 of Tanaka along with the corresponding text in column 8, line 65 – column 9, line 60. Applicant respectfully disagrees.

Tanaka clearly states in column 9, lines 9 – 15, that the row 31a is set at a different pitch as compared to rows 31b and 31c because no wires are connected to 31b or 31c. The pads in rows 31b and 31c as shown in Figure 9 are at the **same** pitch. While row 31a of Tanaka is pitched differently from row 31b, the pitch between rows 31b and 31c are the same. Therefore, Tanaka does not show or suggest pads "situated in rows with **every other row** having a bond pad pitch different than that of ...an **adjacent**

row". Furthermore, Rows 31b and 31c are functional test terminals and, as defined by Tanaka, it is unnecessary to connect any bonding wire directly thereto (see Tanaka, col. Col. 9, lines 14 – 15). Therefore, there would be no reason to arrange rows of functional test terminals (31b, 31c) at different pitches as claimed in the present invention because there is no reason to connect or route bonding wires to the functional test terminals in Tanaka. Thus, it would not be obvious to include "a plurality of die bond pads situatuated on said die wherein said die bond pads are situated in rows with every other row having a bond pad pitch different than that of a bond pad pitch of an adjacent row" as recited in the present claimed invention. The result of the claimed arrangement of "die bond pads" is multiple route lines between rows which is able to allow there to be less layers on a mating PCB (application, page 5, lines 8 – 10). Tanaka does not provide any common problem recognition. In fact, Tanaka does not contemplate connection of wires to the pads in rows 31b and 31c so it would not be obvious to arrange them in the manner claimed in the present claimed invention.

The embodiment shown in Figures 9 and 10 of Tanaka are provided specifically to allow for these functional test terminals to be in place in order to test the working of the internal circuits of the multiple functions of the LSI's (see col. 8, lines 25 – 34). Therefore, there is no need for Tanaka to include a plurality pads situated as in the claimed arrangement because the functional test terminals (31b, 31c) do not require routing lines as intended in the die bond configuration of the present claimed invention. In fact, Tanaka teaches against the configuration set forth in the present claimed invention because Tanaka explicitly says that "it is unnecessary to connect bonding wires to the functional test terminals" (see col. 9, lines 14 – 15). Therefore, the routing of any wires is not a concern of the Tanaka circuit. Rather, Tanaka is concerned with connecting the outermost layer of pads to external circuits and not routing multiple lines to rows of pads as in the present claimed invention. Therefore, there is no motivation to combine Tanaka with Yamada. Additionally, any combination of the devices disclosed by Yamada and/or Tanaka would not produce the present claimed "integrated circuit die for a flip chip" as recited in the present claimed invention.

As claims 2-5, 9-12 and 16-19, are dependant on independent claims 1, 8 and 15, it is respectfully submitted that they are allowable for the same reasons as discussed above regarding claims 1, 8 and 15. In view of the above remarks it is respectfully submitted that claims 1-5, 8-12 and 15-19 are allowable.

In view of the above remarks and amendments to the claims it is respectfully submitted that there is no 35 USC 112 compliant enabling disclosure in Yamada et al. showing the above discussed features. It is thus further respectfully submitted that claims 1-5, 8-12 and 15-19 are not anticipated by Yamada et al. It is thus, further respectfully submitted that this rejection is satisfied and should be withdrawn.

The applicant respectfully submits, in view of the above arguments and the telephone interview of December 4, 2006, that the all arguments made by the Examiner have been addressed and this rejection should be withdrawn. Therefore, the applicant respectfully submits that the present claimed invention is patentable.

No fee is believed due. However, if a fee is due, please charge the additional fee to Deposit Account 07-0832.

Respectfully submitted,
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Date: December 8, 2006

Jack Schwartz